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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,612	10/24/2003	Scott Lee	3304.2.94	6479

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EXAMINER	
KO, DANIEL BOKMIN	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,612	LEE, SCOTT	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 10/24/2003. Claims 1-20 have been submitted for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-6, 8-13, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Roussel et al. (US Patent 6,721,866), hereinafter simply Roussel.

Regarding claims 1 and 9, Roussel teaches a data access method, comprising a data reading procedure to read a certain bit range of data from a data storage zone, said certain bit range being stored in said data storage zone from a starting bit address (a) to an end bit address (b), and said data reading procedure comprising steps of:

performing a first operation of said starting bit address (a) to obtain a first shift S1 (Fig. 5, step 108; column 6, lines 31-34);

performing a second operation of said starting bit address (a) to obtain a second shift S2 (Fig. 5, step 112; column 6, lines 35-38);

performing a first shift operation of said data with said first shift S1 to obtain a first shifted data unit (Fig. 4B, OP1; Fig. 5, Step 110; column 5, lines28-31);

performing a second shift operation of said data with said second shift S2 to obtain a second shifted data unit (Fig. 4B, OP3; Fig. 5, Step 114; column 5, lines 31-34) and

synthesizing said first and said second shifted data units to obtain a read data unit (Fig. 5, Step 118; column 5, lines 35-36; column 6, lines 40-42).

Regarding claims 2 and 10, Roussel teaches a data access method wherein said data storage zone stores data as at least one data unit consisting of m bits, and said bit range consists of n bits, where n is greater than m (Fig. 3, column 3, lines 34-41, column 4, lines 15-24).

Regarding claims 3 and 11, Roussel teaches a data access method wherein said first and said second operations are performed by the following formulae:
S1 = mod [a, m] (column 4, lines 47-49; column 5, lines 28-30); and
S2 = m – mod [a, m] = m – S1 (column 4, lines 52-55; column 5, lines 31-34),
where mod [a, m] is the remainder on division of a by m.

Regarding claims 4 and 12, Roussel teaches a data access method wherein said first shift operation is performed by shifting a first data unit of said data to be read toward one of the higher bit direction (column 4, lines 47-49; column 5, lines 28-30) and

the lower bit direction, and said second shift operation is performed by shifting a second data unit of said data to be read toward the other of the higher bit direction and the lower bit direction (column 4, lines 52-55; column 5, lines 31-34).

Regarding claims 5 and 13, Roussel teaches a data access method according to claim 4 wherein said second data unit is immediately adjacent to said first data unit in said data storage zone (Fig 4B, X operand starts from XX00 to XX12).

Regarding claims 6 and 15, Roussel teaches a data access method wherein said first and said second shift operations are further performed on subsequent data units until a data unit comprising said end data bit address (b) has been shifted to obtain a last shifted data unit (column 5, lines 50-53).

Regarding claims 8 and 17, Roussel teaches a data access method wherein said first and said second shifted data units are synthesized via an OR gate operation (column 5, lines 35-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 7, 14, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roussel et al. (US Patent 6,721,866) in view of Debes et al. (US Patent Application 2003/0084082 A1), hereinafter simply Debes.

Regarding claims 7 and 14, Roussel teaches a data access method, comprising a data reading procedure to read a certain bit range of data from a data storage zone (See claim 1 rejection). Roussel fails to teach a mask data MD for clearing bits excluded from said bit range.

Debes teaches a data access method further comprising a step of masking said last shifted data unit with a mask data MD for clearing bits excluded from said bit range,

where MD=0xFF >> (m-(b-a+1)), the expression "0xFF" indicates an 8-bit hexadecimal mask data and the 8 bits are all "1", and the expression "X >> Y" indicates the rightward shift of the data X by Y bits (Fig. 5, mask 402, paragraphs 55, 56, 72, and 73).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Roussel with Debes. The motivation for doing so would have been an avoiding unnecessary data type change which results in maximizes the number of operations per instruction while reducing the number of clock cycles required to order data for arithmetic operations (See Debes, paragraphs 8 and 92). Also, Roussel's invention can clear the unnecessary bits by using Debes's masking method.

Regarding claim 16, Roussel teaches a data access method, comprising a data reading procedure to read a certain bit range of data from a data storage zone (See claim 1 rejection). Roussel fails to teach a mask data MD for clearing bits excluded from said bit range.

Debes teaches a data access method comprising steps of: performing a third shifting operation of a starting data unit of said data to be written with said first shift S3 (paragraph 70); and

masking said staring data unit with a mask data MD2 for clearing bits excluded from said bit range (Fig. 5, mask 402, paragraphs 55, 56, 72, and 73),

where MD2 = ~(0xFF << S3), the expression "0xFF" indicates an 8-bit hexadecimal mask data and the 8 bits are all "1", the expression "X << Y" indicates the

leftward shift of the data X by Y bits, and the expression "~Z" indicates the reverse logic operation of data Z.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Roussel with Debes. The motivation for doing so would have been an avoiding unnecessary data type change which results in maximizes the number of operations per instruction while reducing the number of clock cycles required to order data for arithmetic operations (See Debes, paragraphs 8 and 92). Also, Roussel's invention can clear the unnecessary bits by using Debes's masking method.

Regarding claim 18, Roussel teaches a data access method, comprising a data reading procedure to read a certain bit range of data from a data storage zone (See claim 1 rejection). Roussel fails to teach a mask data MD for clearing bits excluded from said bit range.

Roussel and Debes teach a data access method, comprising a data writing procedure to write a certain bit range of data into a data storage zone, said data storage zone storing data as at least one data unit consisting of m bits, said certain bit range consisting of n bits and being stored into said data storage zone from a starting bit address (a) to an end bit address (b), and said data writing procedure comprising steps of:

performing a first operation of said starting bit address (a) and said bit number m to obtain a first shift S3 (See Roussel, Fig. 4B, OP1; Fig. 5, Step 110; column 5, lines28-31);

performing a second operation of said starting bit address (a) and said bit number m to obtain a second shift S4 (See Roussel, Fig. 4B, OP3; Fig. 5, Step 114; column 5, lines 31-34);

performing a first clear and writing procedure of said data to be written when n is no greater than m, said first clear and writing procedure comprising a step of masking said data to be written with a first mask data MD1 = ~((0xFF >> ((m-1)-b+a)) << S3) (See Debes, Fig. 5, mask 402, paragraphs 55, 56, 72, and 73);

performing a second clear and writing procedure of said data to be written when n is greater than m, said second clear and writing procedure comprising a step of masking the starting data unit of said data to be written with a second mask data MD2 = ~(0xFF << S3) (See Debes, Fig. 5, mask 402, paragraphs 55, 56, 72, and 73);

performing a third clear and writing procedure of said data to be written when n is greater than m, said third clear and writing procedure comprising a step of masking the end data unit of said data to be written with a third mask data MD3 = 0xFF << (mod [b, m] +1) (See Debes, Fig. 5, mask 402, paragraphs 55, 56, 72, and 73); and

performing a first and a second shift operations of said data with said first and said second shifts S3 and S4 to obtain a first and a second shifted data units, and synthesizing said first and said second shifted data units to obtain a written data unit when n is greater than m (See Roussel, Fig. 5, Step 118; column 5, lines 35-36; column 6, lines 40-42);

where the expression "0xFF" indicates a hexadecimal mask data, the expression "X >> Y" indicates the rightward shift of the data X by Y bits, the expression "X << Y"

indicates the leftward shift of the data X by Y bits, the expression "~Z" indicates the reverse logic operation of data Z, the expression "X & Y" indicates AND gate operation of data X and Y, and the expression "mod [b, m]" indicates the remainder on division of b by m.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Roussel with Debes. The motivation for doing so would have been an avoiding unnecessary data type change which results in maximizes the number of operations per instruction while reducing the number of clock cycles required to order data for arithmetic operations (See Debes, paragraphs 8 and 92). Also, Roussel's invention can clear the unnecessary bits by using Debes's masking method.

3. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roussel et al. (US Patent 6,721,866) and Debes et al. (US Patent Application 2003/0084082 A1) and further in view of Hensen et al. (US Patent 4,814,976), hereinafter simply Hensen.

Regarding claims 19 and 20, Roussel combined with Debes teach a data access method, comprising a data reading procedure to read a certain bit range of data from a data storage zone using shifting and masking (See claim 18 rejection). Neither Roussel nor Debes teach a data writing procedures are performed as little endian or big endian.

Hensen teaches a data access method wherein said data writing procedure is performed as little endian or big endian (column 2, lines 66-68; column 6, lines 26-46).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Roussel and Debes with Hensen. The motivation for doing so would have been an loading or storing an unaligned reference in a reduced number of instruction cycle, thereby maintaining a high processing speed (See Hansen, column 2, lines 8-11). Also, combining Roussel and Debes with Hensen allows to handle both little endian and big endian data format.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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